LM3207 650mA Miniature, Adjustable, Step-Down DC-DC Converter for RF Power Amplifiers with Integrated Vref LDO

Check for Samples: LM3207

FEATURES

- **2MHz (typ.) PWM Switching Frequency**
- **Operates from a single Li-Ion cell (2.7V to 5.5V)**
- **Variable Output Voltage (0.8V to 3.6V)**
- **650mA Maximum load capability**
- **High Efficiency (95% Typ at 3.9V_{IN}, 3.4V_{OUT} at 400mA) from internal synchronous rectification**
- **Integrated Vref LDO**
- **Regulated LDO Output up to 10mA max**
- **Fast 3uS Vref LDO On/Off Time**
- **9-pin micro SMD Package**
- **Current Overload Protection**
- **Thermal Overload Protection**

APPLICATIONS

- **Cellular Phones**
- **Hand-Held Radios**
- **RF PC Cards**
- **Battery Powered RF Devices**

DESCRIPTION

The LM3207 is a DC-DC converter optimized for powering WCDMA / CDMA RF power amplifiers (PAs) from a single Lithium-Ion cell; however they may be used in many other applications. It steps down an input voltage from 2.7V to 5.5V to a variable output voltage from 0.8V(typ.) to 3.6V(typ.). Output voltage is set using a V_{CON} analog input for controlling power levels and efficiency of the RF PA.

The LM3207 also provides a regulated reference voltage(Vref) required by linear RF power amplifiers through an integrated LDO that has a maximum Iref up to 10 mA. See Ordering Information table on page 2 for Voltage Options.

The LM3207 is available in a 9-pin lead free micro SMD package. High switching frequency (2MHz) allows use of surface-mount components. Only four small external surface-mount components are required, an inductor and three ceramic capacitors.

Typical Application

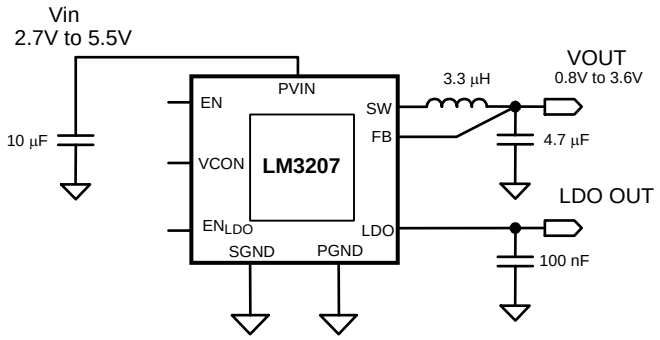

Figure 1. LM3207 Typical Application

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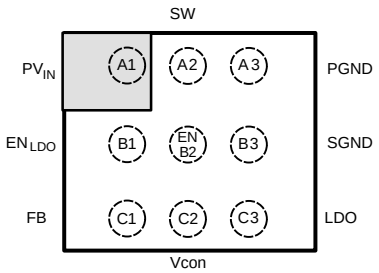
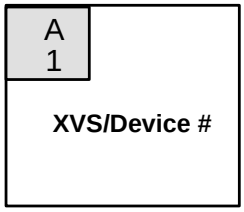
Connection Diagrams



Top View



Package Mark - Top View

9–Bump Thin Micro SMD Package, Large Bump NS Package Number TLA09TTA (1)

Table 1. Pin Descriptions

Pin #	Name	Description
A1	PV_{IN}	Power Supply Voltage Input.
B1	EN_{LDO}	LDO Enable Input. Set this digital input high to turn on LDO (ENpin must also be set high). For shutdown, set low.
C1	FB	Feedback Analog Input. Connect to the output at the output filter capacitor.
C2	V_{CON}	Voltage Control Analog input. V_{CON} controls V_{OUT} in PWM mode.
C3	LDO	LDO Output Voltage.
B3	SGND	Analog and Control Ground.
A3	PGND	Power Ground.
A2	SW	Switch node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3207.
B2	EN	PWM enable Input. Set this digital input high for normal operation. For shutdown, set low.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings [1] [2]

PV_{IN} to SGND	−0.2V to +6.0V
PGND to SGND	−0.2V to +0.2V
EN, FB, V_{CON}, EN_{LDO}, LDO	(SGND −0.2V) to (V_{DD} +0.2V) w/6.0V max
SW	(PGND −0.2V) to (PV_{IN} +0.2V) w/6.0V max
PV_{IN}	−0.2V to +0.2V
Continuous Power Dissipation [3]	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec)	+260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins. The LM3207 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).

Operating Ratings [1] [2]

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	0mA to 650mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range [3]	−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins. The LM3207 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), TLA09 Package [1]	100°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from thermal measurements, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7.

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Electrical Characteristics (1) (2) (3)

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range (−30°C ≤ $T_A = T_J$ ≤ +85°C). Unless otherwise noted, all specifications apply to all LM3207 LDO options with: $PV_{IN} = V_{IN} = EN_{LDO} = EN = 3.6V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LDO						
V_{LDO}	LDO Output Voltage	Iout = 0 mA			**+2.6**	%
$V_{LDO,MIN}$	Minimum LDO Output Voltage	Iout = 10mA, PV_{IN} = 3V	**-2.6**			%
I_{SC}	Short circuit current(DC)	V_{LDO} = 0		50		mA
I_{PUT}	Pull-up current (transient)	$V_{LDO} = V_{LDO(nom)}/2$, PV_{IN} = 3V (4)	150			mA
I_{PD}	DC Pull-down current (DC)	$V_{LDO} = PV_{IN}$, EN_{LDO} = 0		-50		mA
I_{PDT}	Pull-down current (transient)	V_{LDO} = 1.44V, PV_{IN} = 3V (4)			-200	mA
$I_{Q_LDO + PWM}$	DC Bias current into PV_{IN}	V_{CON} = 2V, FB = 0V, No Switching, EN_{LDO} = EN = 3.6V (5)		1.2	**1.6**	mA
$I_{PIN,EN_{LDO}}$	LDO Pin pull down current			5	**10**	uA
Switcher						
$V_{FB, MIN}$	Feedback Voltage at minimum setting	V_{CON} = 0.32V	**0.75**	0.8	**0.85**	V
$V_{FB, MAX}$	Feedback Voltage at maximum setting	V_{CON} = 1.44V, PV_{IN} = 4.2V	**3.537**	3.6	**3.683**	V
I_{SHDN}	Shutdown supply current	EN = EN_{LDO}= SW = V_{CON} = 0V, (6)		0.01	**2**	µA
I_{Q_PWM}	DC bias current into PV_{IN}	V_{CON} = 2V, FB = 0V, EN_{LDO} = 0V , EN = 3.6V, No Switching (5)		1.1	**1.6**	mA
$R_{DSON(P)}$	Pin-pin resistance for PFET	I_{SW} = 200mA		140	200 **230**	mΩ
$R_{DSON(N)}$	Pin-pin resistance for NFET	I_{SW} = - 200mA		300	415 **485**	mΩ
$I_{LIM,PFET}$	Switch peak current limit	(7)	**935**	1100	**1200**	mA
F_{OSC}	Internal oscillator frequency		**1.7**	2	**2.3**	MHz
$V_{IH,EN}$	Logic high input threshold (PWM, LDO)		**1.2**			V
$V_{IL,EN}$	Logic low input threshold (PWM, LDO)				**0.5**	V
$I_{PIN,EN}$	PWM Pin pull down current			5	**10**	µA
Gain	V_{CON} to V_{OUT} Gain	0.32V ≤ V_{CON} ≤ 1.44V		2.5		V/V
I_{CON}	V_{CON} pin leakage current	V_{CON} = 1.0V			**±1**	µA

(1) All voltages are with respect to the potential at the GND pins. The LM3207 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Due to the pulsed nature of the testing $T_A = T_J$ for the electrical characteristics table.
(3) The parameters in the electrical characteristics table are tested under open loop conditions at PV_{IN} = 3.6V. For performance over the input voltage range and closed loop results refer to the datasheet curves.
(4) Transient Pull-up current (I_{PUT}) and Transient Pull-down Current (I_{PDT}) will be tested which are inversely proportional to charge and discharge times $t_{LDO, ON}$ and $t_{LDO, OFF}$ respectively.
(5) I_Q specified here is when the part is operating at 100% duty cycle.
(6) Shutdown current includes leakage current of PFET.
(7) Current limit is built-in, fixed, and not adjustable. Refer to datasheet curves for closed loop data and its variation with regards to supply voltage and temperature. Electrical Characteristic table reflects open loop data (FB = 0V and current drawn from SW pin ramped up until cycle by cycle limit is activated). Closed loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

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System Characteristics

The following spec table entries are guaranteed by design providing the component values in the typical application circuit are used (L = 3.0µH, (DCR = 0.12Ω, FDK MIPW3226D3R0M);
C_{IN} = 10µF, (6.3V, 0805, TDK C2012X5R0J106K); C_{OUT} = 4.7µF, (6.3V, 0603, TDK C1608X5R0J475M); C_{LDO} = 100nF, (10V, 0402, TDK C1005X5R1A104KT) (or 220nF, (6.3V, 0402, TDK C1005X5R0J224KT))) . **These parameters are not guaranteed by production testing.** Min and Max values are specified over the V_{IN} range = 2.7V to 5.5V and over the ambient temp range T_A = −30°C to 85°C unless otherwise specified. Typical values are specified at PV_{IN} = EN = 3.6V and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LDO						
PSRR	Power Supply Rejection Ratio	Offset Freq = 1Khz, C_{out} = 100nF, I_{out} = 1mA, PV_{in} = $Vout_{(nom)}$ + 0.5V		50		dB
$V_{LDO(NOISE)}$	Output Noise Voltage	BW = 10Hz to 100Khz, I_{out} = 1mA		30		uVrms
$t_{LDO, ON}$	Time to reach 90% of $V_{LDO(nom)}$ after EN_{LDO} signal goes high.	C_{LDO} = 100nF, PWM mode assumed to be fully functional before EN_{LDO} goes high. PV_{in} = 3V, R_{LOAD} = 562 Ω (1)			3	uS
		C_{LDO} = 220nF, PWM mode assumed to be fully functional before EN_{LDO} goes high. PV_{in} = 3V, R_{LOAD} = 562 Ω (1)			5	uS
$t_{LDO, OFF}$	Time to reach 10% of $V_{LDO(nom)}$ after EN_{LDO} signal goes low.	C_{LDO} = 100nF, PV_{in} = 3V, Iout = 0mA (1)			3	uS
		C_{LDO} = 220nF, PV_{in} = 3V, Iout = 0mA (1)			5	
Switcher						
$T_{RESPONSE}$ (Rise time)	Time for V_{OUT} to rise from 0.8V to 3.6V	PV_{IN} = 4.2V, C_{OUT} = 4.7uF, L = 3.0uH, R_{LOAD} = 5.5Ω		20	30	µs
$T_{RESPONSE}$ (Fall time)	Time for V_{OUT} to fall from 3.6V to 0.8V	PV_{IN} = 4.2V, C_{OUT} = 4.7uF, L = 3.0uH, R_{LOAD} = 10Ω		20	30	µs
C_{CON}	V_{CON} input capacitance	V_{CON} = 1V, Test frequency = 100 kHz			20	pF
V_{CON} Linearity	Linearity in control range 0.32V to 1.44V	PV_{IN} = 3.9V, Monotonic in nature	-3		+3	%
$T_{_ON}$	Turn on time (time for output to reach 3.6V from Enable low to high transition)	EN = Low to High, PV_{IN} = 4.2V, V_O = 3.6V, C_{OUT} = 4.7µF, I_{OUT} ≤ 1mA		70	100	µs
η	Efficiency (L = 3.0µH, DCR ≤ 100mΩ)	PV_{IN} = 3.6V, V_{OUT} = 0.8V, I_{OUT} = 90mA		81		%
		PV_{IN} = 3.9V, V_{OUT} = 3.4V, I_{OUT} = 400mA		95		%
V_{O_ripple}	Ripple voltage, PWM mode	PV_{IN} = 3V to 4.5V, V_{OUT} = 0.8V, I_{OUT} = 10mA to 400mA, (2)		10		mVp-p
Line_tr	Line transient response	PV_{IN} = 600mV perturbance, T_{RISE} = T_{FALL} = 10µs, V_{OUT} = 0.8V, I_{OUT} = 100mA		50		mV
Load_tr	Load transient response	PV_{IN} = 3.1/3.6/4.5V, V_{OUT} = 0.8V, transients up to 100mA, T_{RISE} = T_{FALL} = 10µs		50		mV

(1) Transient Pull-up current (I_{PUT}) and Transient Pull-down Current (I_{PDT}) will be tested which are inversely proportional to charge and discharge times $t_{LDO, ON}$ and $t_{LDO, OFF}$ respectively.
(2) Ripple voltage should measured at C_{OUT} electrode on good layout PC board and under condition using suggested inductors and capacitors.

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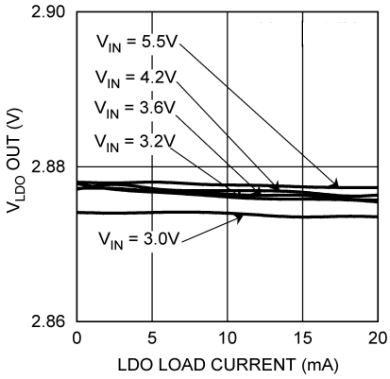
Typical Performance Characteristics

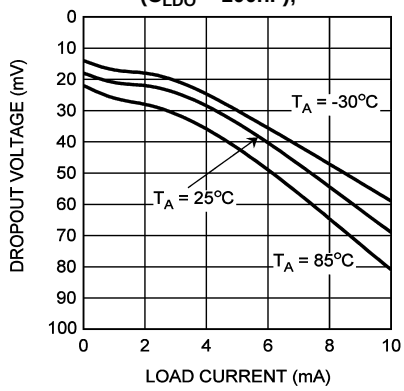
(Circuit in Figure 3, See Operation Description Section),
PV_{IN} = EN = 3.6V, L = 3.0µH, (DCR = 0.12Ω, FDK MIPW3226D3R0M); C_{IN} = 10µF, (6.3V, 0805, TDK C2012X5R0J106K); C_{OUT} = 4.7µF, (6.3V, 0603, TDK C1608X5R0J475M), C_{LDO} = 100nF, 10V, (0402, TDK C1005X5R1A104KT) (or 220nF, (6.3V, 0402, TDK C1005X5R0J224KT)) can be used. T_A = 25°C unless otherwise specified.

LDO Typical Performance Curves (2.875 Option)

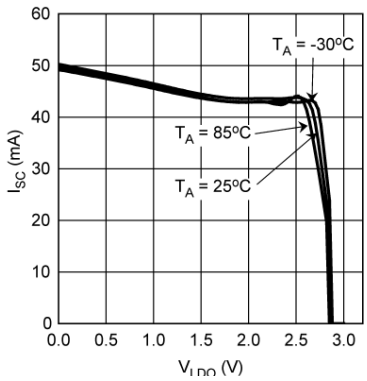
LDO Voltage vs Load Current (C_{LDO} = 100nF)



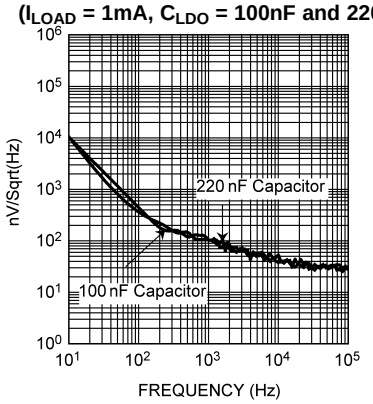
LDO Dropout Voltage vs Load Current (C_{LDO} = 100nF), (1)



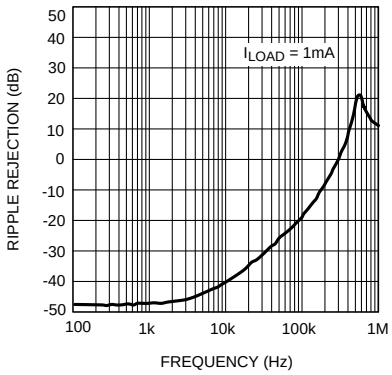
LDO Short Circuit Current vs Voltage (V_{IN} = 3.0V, C_{LDO} = 100nF)



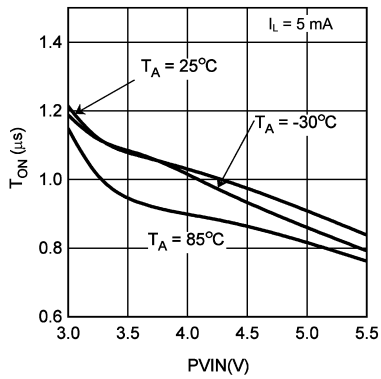
LDO Output Noise Density (I_{LOAD} = 1mA, C_{LDO} = 100nF and 220nF)



LDO Power Supply Rejection Ratio (V_{IN} = $Vout_{(nom)}$ + 0.5V, C_{LDO} = 100nF)



LDO Turn On Time vs V_{IN} (C_{LDO} = 100nF)



(1) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

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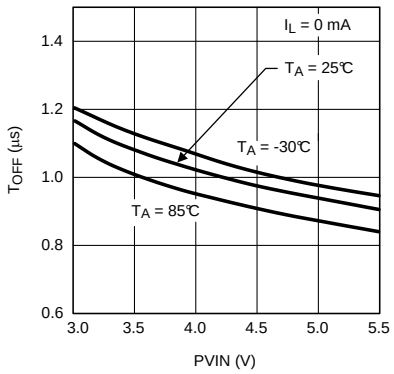
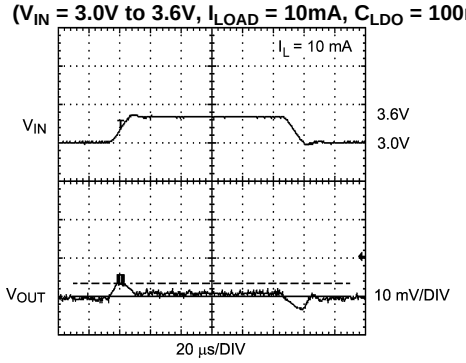
LDO Typical Performance Curves (2.875 Option) (continued)

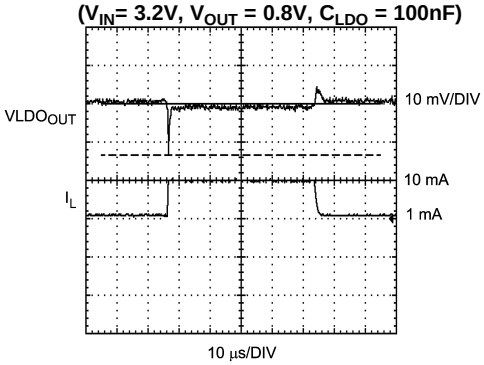
LDO Turn Off Time vs V_{IN} (C_{LDO} = 100nF)



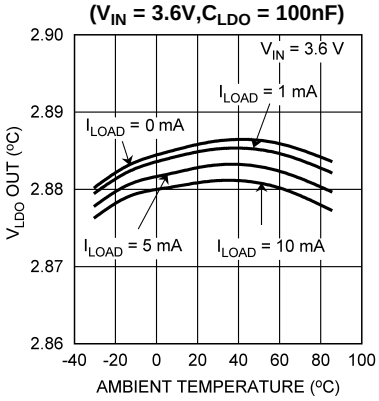
LDO Line Transient Response (V_{IN} = 3.0V to 3.6V, I_{LOAD} = 10mA, C_{LDO} = 100nF)



LDO Load Transient Repsonse (V_{IN}= 3.2V, V_{OUT} = 0.8V, C_{LDO} = 100nF)

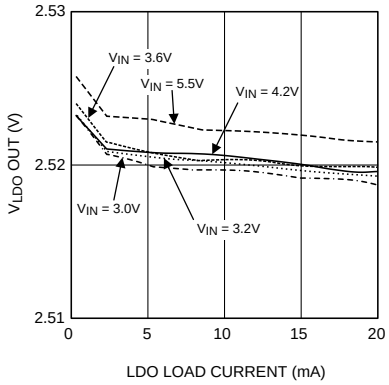


LDO V_{LDO} Out vs Temperature (V_{IN} = 3.6V,C_{LDO} = 100nF)

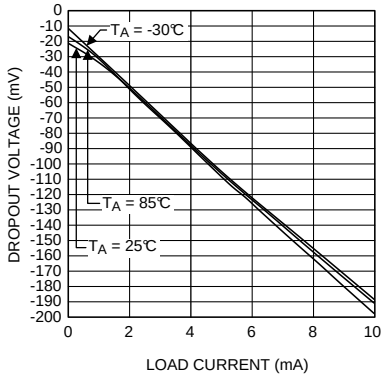


LDO Typical Performance Curves (2.53 Option)

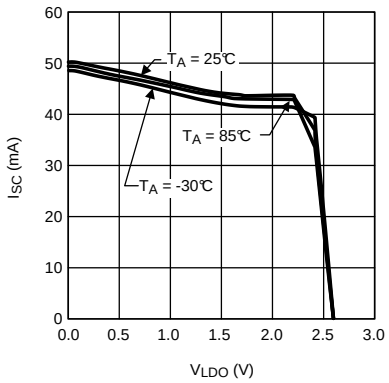
LDO Voltage vs Load Current (C_{LDO} = 100nF)



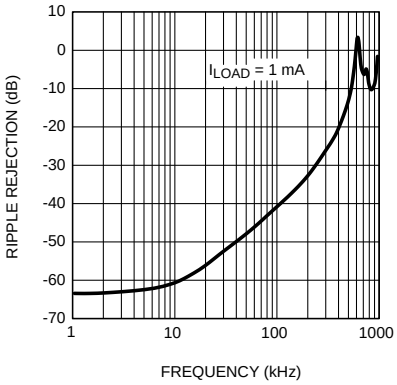
LDO Dropout Voltage vs Load Current (C_{LDO} = 100nF), (1)



LDO Short Circuit Current vs Voltage (V_{IN} = 3.0V, C_{LDO} = 100nF)



LDO Power Supply Rejection Ratio (V_{IN} = $Vout_{(nom)}$ + 0.5V, C_{LDO} = 100nF)



(1) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

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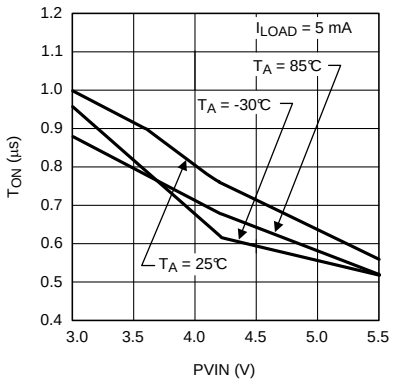
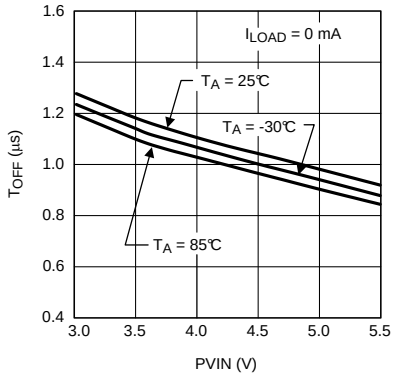
LDO Typical Performance Curves (2.53 Option) (continued)

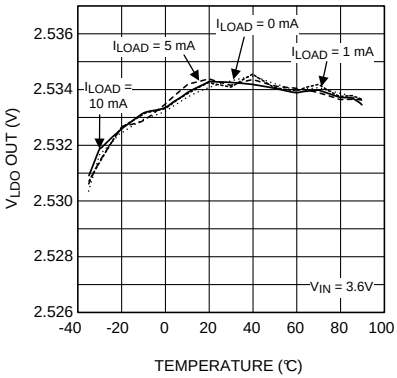
LDO Turn On Time vs V_{IN} (C_{LDO} = 100nF)



LDO Turn Off Time vs V_{IN} (C_{LDO} = 100nF)

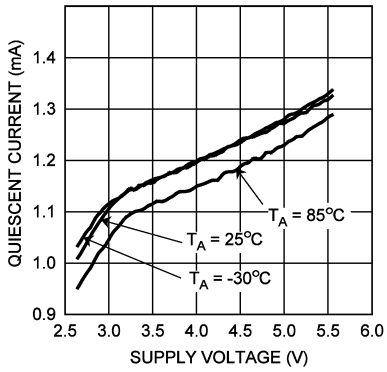


LDO V_{LDO} Out vs Temperature (V_{IN} = 3.6V,C_{LDO} = 100nF)

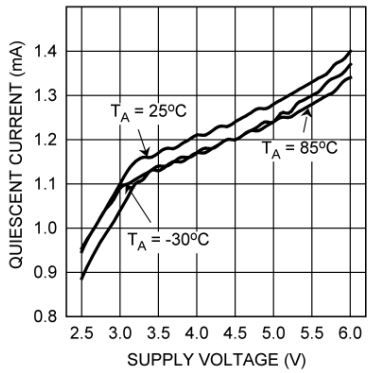


SWITCHER Typical Performance Curves

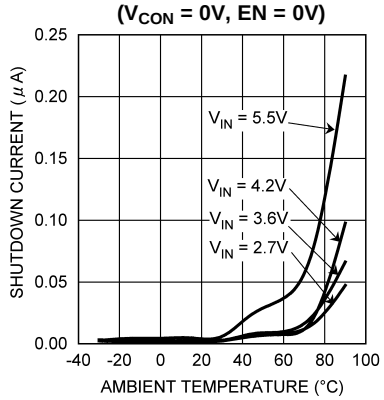
Quiescent Current vs Supply Voltage (V_{CON} = 2V, FB = 0V, No Switching, LDO Disabled)



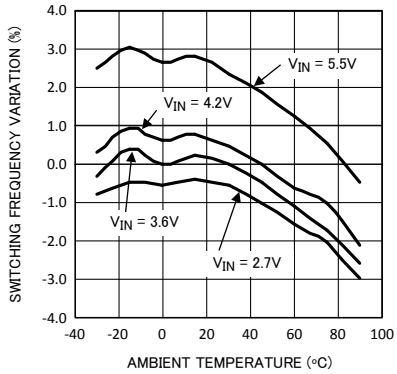
Quiescent Current vs Supply Voltage (V_{CON} = 2V, FB = 0V, No Switching, LDO Enabled)



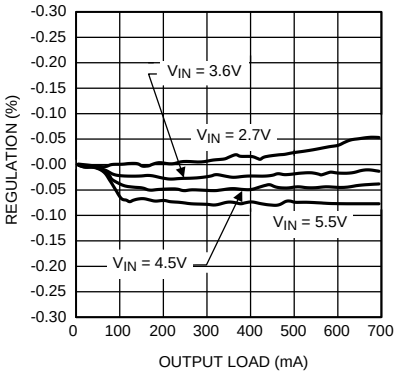
Shutdown Current vs Temperature (V_{CON} = 0V, EN = 0V)



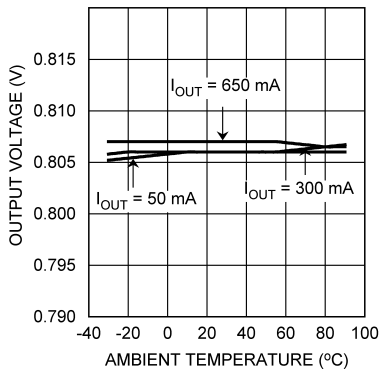
Switching Frequency vs Temperature (V_{OUT} = 1.3V, I_{OUT} = 200mA)



Output Voltage Regulation(%) vs Output Load (V_{OUT} = 1.5V)



Output Voltage vs Temperature (V_{IN} = 3.6V, V_{OUT} = 0.8V)



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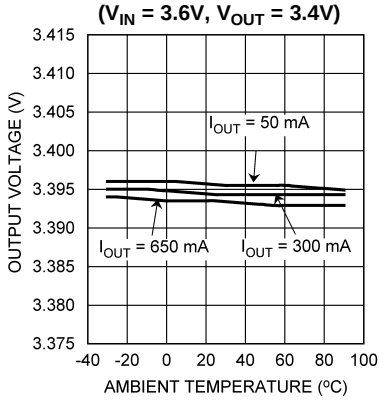
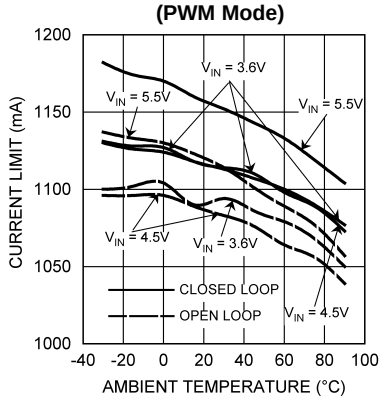
SWITCHER Typical Performance Curves (continued)

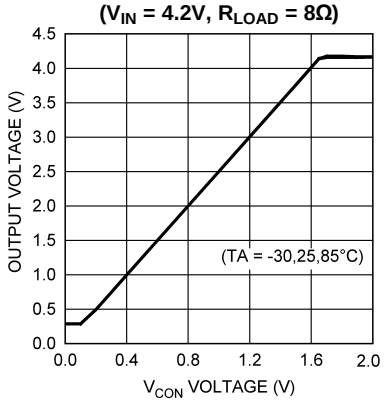
Output Voltage vs Temperature (V_{IN} = 3.6V, V_{OUT} = 3.4V)



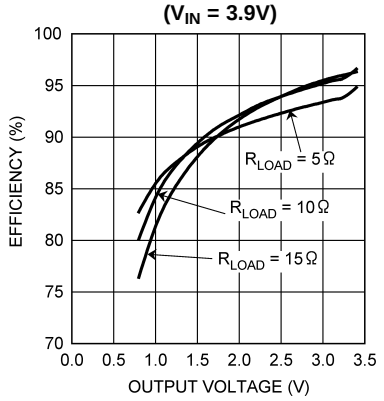
Open/Closed Loop Current Limit vs Temperature (PWM Mode)



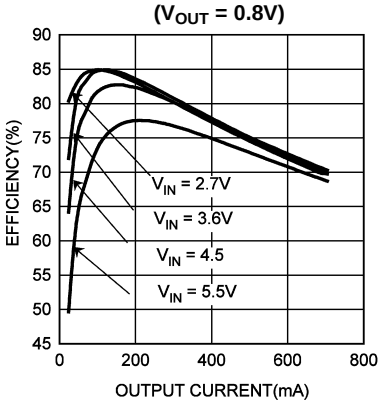
V_{CON} Voltage vs Output Voltage (V_{IN} = 4.2V, R_{LOAD} = 8Ω)



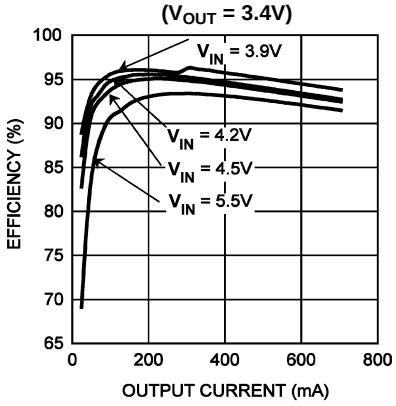
Efficiency vs Output Voltage (V_{IN} = 3.9V)



Efficiency vs Output Current (V_{OUT} = 0.8V)

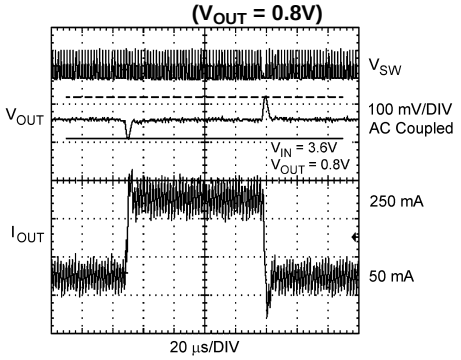


Efficiency vs Output Current (V_{OUT} = 3.4V)

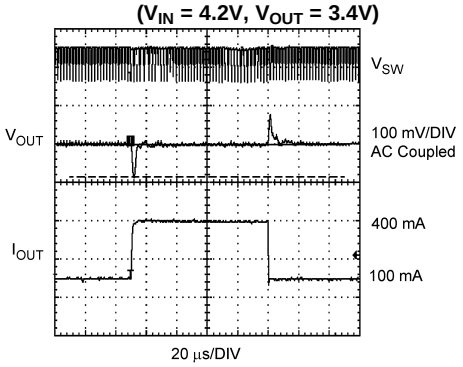


SWITCHER Typical Performance Curves (continued)

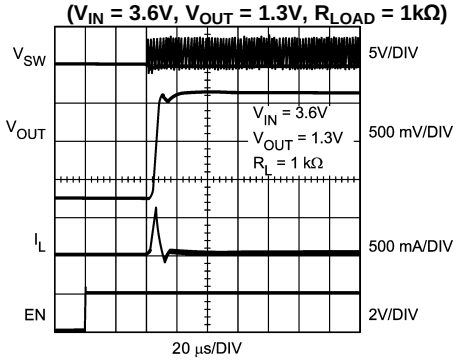
Load Transient Response (V_{OUT} = 0.8V)



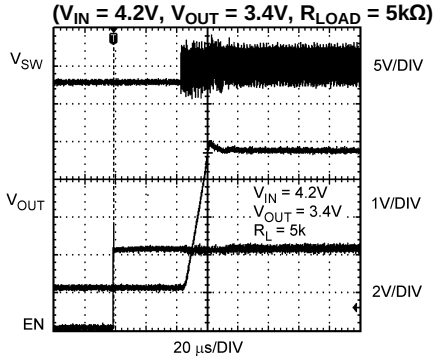
Load Transient Response (V_{IN} = 4.2V, V_{OUT} = 3.4V)



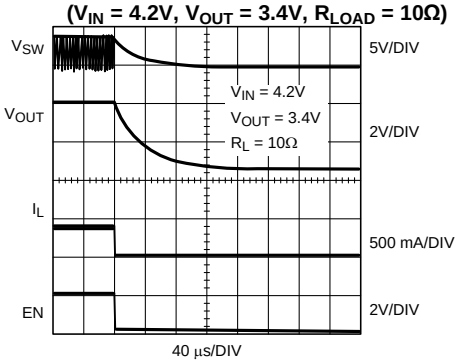
Startup (V_{IN} = 3.6V, V_{OUT} = 1.3V, R_{LOAD} = 1kΩ)



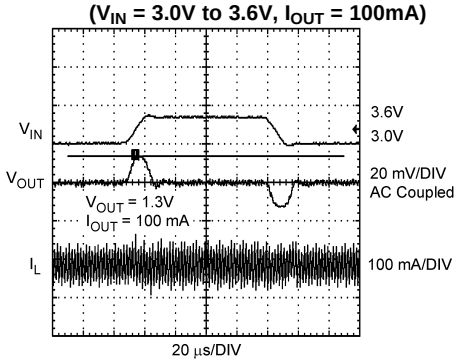
Startup (V_{IN} = 4.2V, V_{OUT} = 3.4V, R_{LOAD} = 5kΩ)



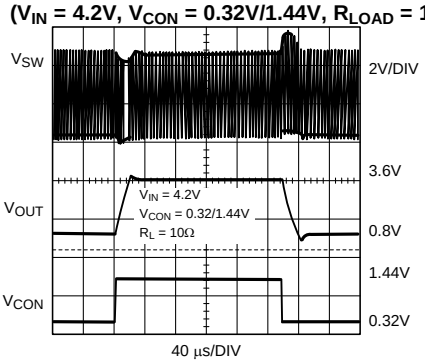
Shutdown Response (V_{IN} = 4.2V, V_{OUT} = 3.4V, R_{LOAD} = 10Ω)



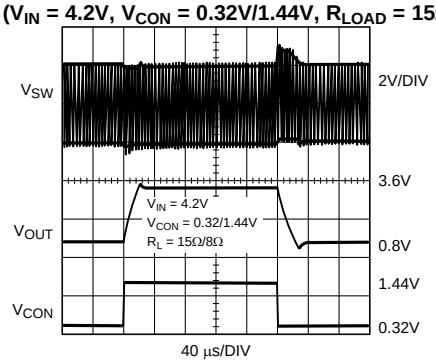
Line Transient Reponse (V_{IN} = 3.0V to 3.6V, I_{OUT} = 100mA)



V_{CON} Voltage Response (V_{IN} = 4.2V, V_{CON} = 0.32V/1.44V, R_{LOAD} = 10Ω)



V_{CON} and Load Transient (V_{IN} = 4.2V, V_{CON} = 0.32V/1.44V, R_{LOAD} = 15Ω/8Ω)



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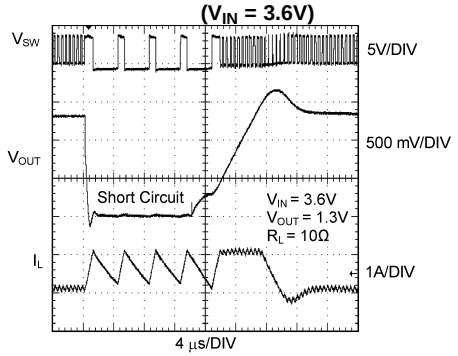
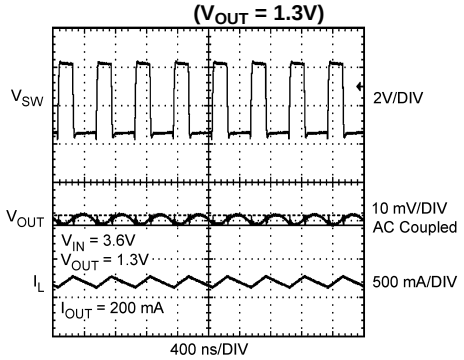
SWITCHER Typical Performance Curves (continued)

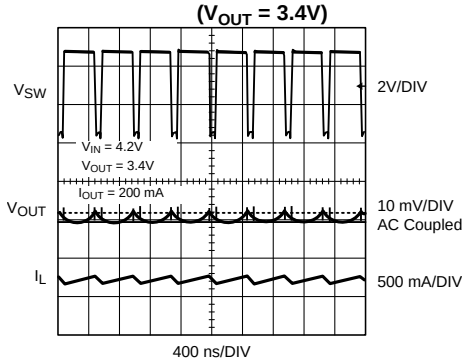
Timed Current Limit Response
(V_{IN} = 3.6V)



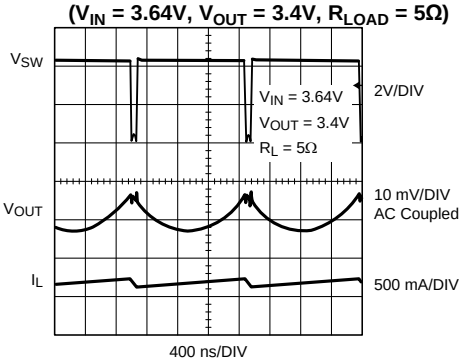
Output Voltage Ripple
(V_{OUT} = 1.3V)



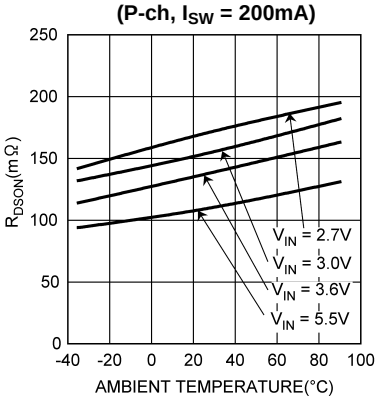
Output Voltage Ripple
(V_{OUT} = 3.4V)



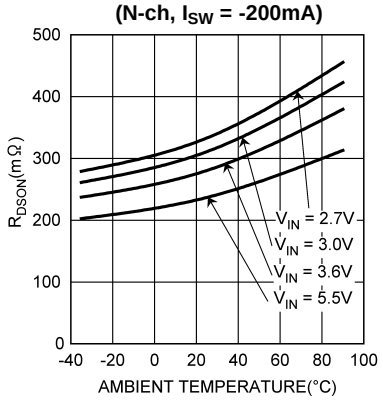
Output Voltage Ripple in Pulse Skip
(V_{IN} = 3.64V, V_{OUT} = 3.4V, R_{LOAD} = 5Ω)



R_{DSON}
vs
Temperature (microSMD)
(P-ch, I_{SW} = 200mA)



R_{DSON}
vs
Temperature (microSMD)
(N-ch, I_{SW} = -200mA)



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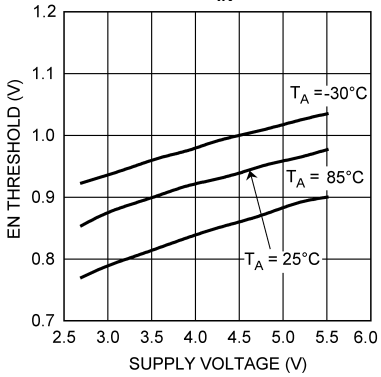
SWITCHER Typical Performance Curves (continued)

EN High Threshold
vs
V_{IN}



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Block Diagram

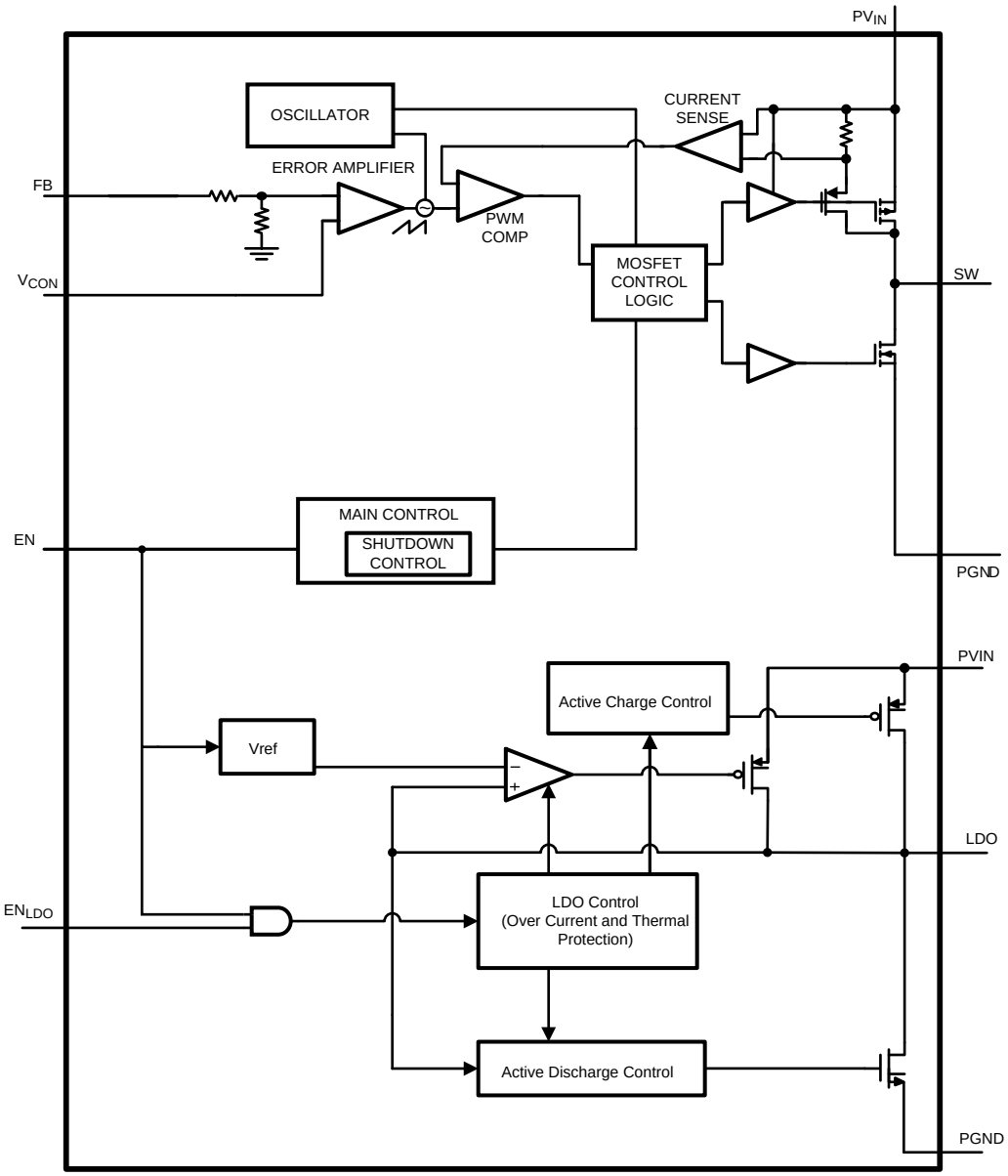

Figure 2. Functional Block Diagram

Operation Description

The LM3207 is a simple, step-down DC-DC converter with a VREF LDO optimized for powering RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery powered RF devices. The DC-DC converter is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels from a single Lithium-Ion battery cell. The DC-DC is based on current-mode buck architecture, with synchronous rectification for high efficiency. It is designed for a maximum load capability of 650mA in PWM mode.

Maximum load range may vary from this depending on input voltage, output voltage and the inductor chosen.

The device has two pin-selectable operating modes required for powering RF PAs in mobile phones and other sophisticated portable devices. Fixed-frequency PWM operation offers regulated output at high efficiency while minimizing interference with sensitive IF and data acquisition circuits. Shutdown mode turns the device off and reduces battery consumption to 0.01uA (typ).

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Efficiency is typically around 95% for a 400mA load with $3.9V_{IN}$, $3.4V_{OUT}$. The output voltage is dynamically programmable from 0.8V (typ) to 3.6V (typ) by adjusting the voltage on the control pin without the need for external feedback resistors. This ensures longer battery life by being able to change the PA supply voltage dynamically depending on its transmitting power.

Additional features include current overload protection, and thermal overload shutdown.

The LM3207 is constructed using a chip-scale 9-pin micro SMD package. This package offers the smallest possible size, for space-critical applications such as cell phones, where board area is an important design consideration. Use of a high switching frequency (2MHz) reduces the size of external components. As shown in Figure 1, only four external power components are required for implementation. Use of a micro SMD package requires special design considerations for implementation. (See Micro SMD Package Assembly and use in the Applications Information section.) The fine bump-pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also, the system controller should set EN low during power-up and other low supply voltage conditions. (See Shutdown Mode in the Device Information section.)

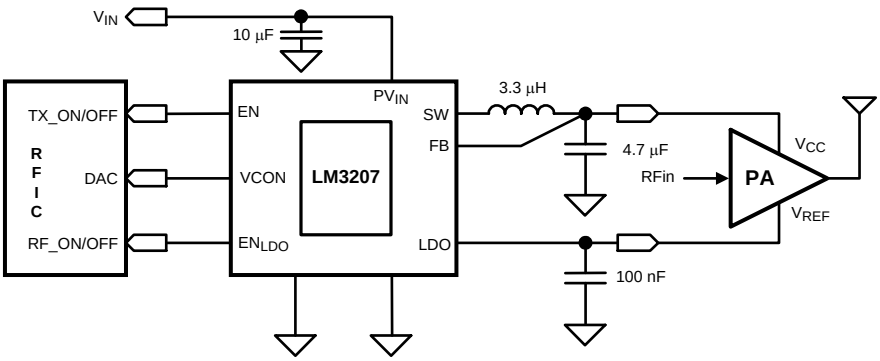

Figure 3. Typical Application Circuit

Circuit Operation (DC-DC Converter)

Referring to Figure 1 and Figure 2, the LM3207 operates as follows. During the first part of each switching cycle, the control block in the LM3207 turns on the internal PFET (P-channel MOSFET) switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around (PV_{IN} - V_{OUT}) / L, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET (N-channel MOSFET) synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around V_{OUT} / L. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

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PWM Operation

While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse width to control the peak inductor current. This is done by comparing the signal from the current-sense amplifier with a slope compensated error signal from the voltage-feedback error amplifier. At the beginning of each cycle, the clock turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator turns off the PFET switch and turns on the NFET synchronous rectifier, ending the first part of the cycle. If an increase in load pulls the output down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET. This increases the average current sent to the output and adjusts for the increase in the load. Before appearing at the PWM comparator, a slope compensation ramp from the oscillator is subtracted from the error signal for stability of the current feedback loop. The minimum on time of PFET in PWM mode is 50ns (typ.)

Shutdown Mode

Setting the EN digital pin low (<0.5V) places the LM3207 in a 0.01µA (typ.) Shutdown mode. During shutdown, the PFET switch, NFET synchronous rectifier, reference voltage source, control and bias circuitry of theLM3207 are turned off. Setting EN high (>1.2V) enables normal operation.

EN should be set low to turn off the LM3207 during power-up and under voltage conditions when the power supply is less than the 2.7V minimum operating voltage. The LM3207 is designed for compact portable applications, such as mobile phones. In such applications, the system controller determines power supply sequencing and requirements for small package size outweigh the additional size required for inclusion of UVLO (Under Voltage Lock-Out) circuitry.

Internal Synchronous Rectification

While in PWM mode, the LM3207 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across and ordinary rectifier diode.

The internal NFET synchronous rectifier is turned on during the inductor current down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

Current Limiting

A current limit feature allows the LM3207 to protect itself and external components during overload conditions. In PWM mode, a 1200mA (max.) cycle-by-cycle current limit is normally used. If an excessive load pulls the output voltage down to approximately 0.375V, then the device switches to a timed current limit mode. In timed current limit mode the internal PFET switch is turned off after the current comparator trips and the beginning of the next cycle is inhibited for 3.5us to force the instantaneous inductor current to ramp down to a safe value. The synchronous rectifier is off in timed current limit mode. Timed current limit prevents the loss of current control evident in some products when the output voltage is pulled low in serious overload conditions.

Dynamically Adjustable Output Voltage

The LM3207 features dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.8V(typ.) to 3.6V(typ.) by changing the voltage on the analog V_{CON} pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life. See *Setting the Output Voltage* in the *Application Information section* for further details.

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Thermal Overload Protection

The LM3207 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds 150°C, the device inhibits operation. The PFET and NFET are turned off in PWM mode. The LDO is turned off as well. When the temperature drops below 130°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

LDO Operation

An LDO is used to provide a regulated Vref supply to a RF PA with a fixed voltage. The LDO can be enabled only after the PWM is running. The LDO will automatically be disabled whenever the EN or EN_{LDO} is disabled. Included in the LDO are active charge and discharge circuits to quickly move a 100nF capacitor to meet the 3us timing requirements, or an 220nF capacitor to meet the 5us timing requirements. The charging and discharging currents are controlled to minimize supply disturbances. The LM3207 was designed specifically to work with a 100nF or a 220nF ceramic capacitor and no bypass capacitor. See Ordering Information table on page 2 for Voltage Options.

Application Information

SETTING THE DC-DC CONVERTER OUTPUT VOLTAGE

The LM3207 features a pin-controlled variable output voltage to eliminate the need for external feedback resistors. It can be programmed for an output voltage from 0.8V (typ.) to 3.6V (typ.) by setting the voltage on the V_{CON} pin, as in the following formula:

$$V_{OUT} = 2.5 \times V_{CON} \quad (2)$$

When V_{CON} is between 0.32V and 1.44V, the output voltage will follow proportionally by 2.5 times of V_{CON}.

If V_{CON} is over 1.44V (V_{OUT} = 3.6V), sub-harmonic oscillation may occur because of insufficient slope compensation. If V_{CON} voltage is less than 0.32V (V_{OUT} = 0.8V), the output voltage may not be regulated due to the required on-time being less than the minimum on-time (50ns). The output voltage can go lower than 0.8V providing a limited V_{IN} range is used. Refer to datasheet curve (V_{CON} Voltage vs Output Voltage) for details. This curve is for a typical part and there could have part-to-part variation for output voltages less than 0.8V over the limited V_{IN} range.

LDO CAPACITOR SELECTION

The output capacitor should be connected between the LDO output and a good ground connection. This capacitor must be selected within specified capacitance range and have sufficiently low ESR. The ESR of the capacitor is generally a major factor in LDO stability. Refer to manufacturer ESR curves for more detail. Table 2 suggests acceptable capacitors and their suppliers.

Table 2. Suggested capacitors and their suppliers

Model	Vendor
C1005X5R1A104KT, 100nF, 10V	TDK
C1005X5R0J224KT, 220nF, 6.3V	TDK

INDUCTOR SELECTION

A 3.3µH inductor with saturation current rating over 1200mA and low inductance drop at the full DC bias condition is recommended for almost all applications. The inductor's DC resistance should be less than 0.2Ω for good efficiency. For low dropout voltage, lower DCR inductors are advantageous. The lower limit of acceptable inductance is 1.7µH at 1200mA over the operating temperature range. Full attention should be paid to this limit, because some small inductors show large inductance drops at high DC bias. These can not be used with the LM3207. Table 3 suggests some inductors and suppliers.

Table 3. Suggested inductors and their suppliers

Model	Size (WxLxH) [mm]	Vendor
NR3015T3R3M	3.0 x 3.0 x 1.5	Taiyo-Yuden

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Table 3. Suggested inductors and their suppliers (continued)

Model	Size (WxLxH) [mm]	Vendor
DO3314-332MXC	3.3 x 3.3 x 1.4	Coilcraft
MIPW3226D3R0M	3.2 x 2.6 x 1.0	FDK

If a smaller inductance inductor is used in the application, the LM3207 may become unstable during line and load transients and V_{CON} transient response times may be affected. For low-cost applications, an unshielded bobbin inductor is suggested. For noise critical applications, a toroidal or shielded-bobbin inductor is recommended. A good practice is to layout the board with footprints accommodating both types for design flexibility. This allows substitution of a low-noise toroidal inductor, in the event that noise from low-cost bobbin models is unacceptable. Saturation occurs when the magnetic flux density from current through the windings of the inductor exceeds what the inductor's core material can support with a corresponding magnetic field. This can result in poor efficiency, regulation errors or stress to DC-DC converter like the LM3207.

DC-DC CONVERTER CAPACITOR SELECTION

The LM3207 is designed with a ceramic capacitor for its input and output filters. Use a 10µF ceramic capacitor for input and a 4.7µF ceramic capacitor for output. They should maintain at least 50% capacitance at DC bias and temperature conditions. Ceramic capacitors types such as X5R, X7R are recommended for both filters. These provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. Table 4 lists suggests acceptable part numbers and their suppliers. DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. If it is necessary to choose a 0603-size capacitor for V_{IN}, the operation of the LM3207should be carefully evaluated on the system board. Output capacitors with smaller case sizes mitigate piezo electric vibrations when the output voltage is stepped up and down at fast rates. However, they have a larger percentage drop in value with dc bias. Use of multiple 2.2µF or 1µF capacitors in parallel may also be considered.

Table 4. Suggested capacitors and their suppliers

Model	Vendor
0805ZD475KA, 4.7µF, 10V	Taiyo-Yuden
C1608X5R0J475M, 4.7uF, 6.3V	TDK
C1608X5R0J106M, 10µF, 6.3V	TDK
C2012X5R0J106M, 10uF, 6.3V	TDK
C2012X5R1A475M, 4.7uF, 6.3V	TDK

The input filter capacitor supplies AC current drawn by the PFET switch of the LM3207 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a factor in voltage ripple.

EN PIN CONTROL

Drive the EN and EN_{LDO} pins using the system controller to turn the LM3207 ON and OFF. Use a comparator, Schmidt trigger or logic gate to drive the EN and EN_{LDO} pins. Set EN high (>1.2V) for normal operation and low (<0.5V) for a 0.01µA (typ.) shutdown mode.

Set EN low to turn off the LM3207 during power-up and under voltage conditions when the power supply is less than the 2.7V minimum operating voltage. The part is out of regulation when the input voltage is less than 2.7V. The LM3207 is designed for mobile phones where the system controller controls operation mode for maximizing battery life and requirements for small package size outweigh the additional size required for inclusion of UVLO (Under Voltage Lock-Out) circuitry.

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Micro SMD PACKAGE ASSEMBLY AND USE

Use of the Micro SMD package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in National Semiconductor Application Note 1112. Refer to the section Surface Mount Technology (SMD) Assembly Considerations. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with Micro SMD package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 for specific instructions.

The 9-Bump package used for LM3207 has 300 micron solder balls and requires 10.82mil pads for mounting the circuit board. The trace to each pad should enter with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 6-7mil wide, for a section approximately 6mil long or longer, to provide thermal relief. Each trace should then neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1, A3 and B3. Because P_{GND} and PV_{IN} are typically connected to large copper planes, inadequate thermal relief's may result in late or inadequate re-flow of these bumps. The Micro SMD package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the Micro SMD package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metalization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. Micro SMD devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

BOARD LAYOUT CONSIDERATIONS

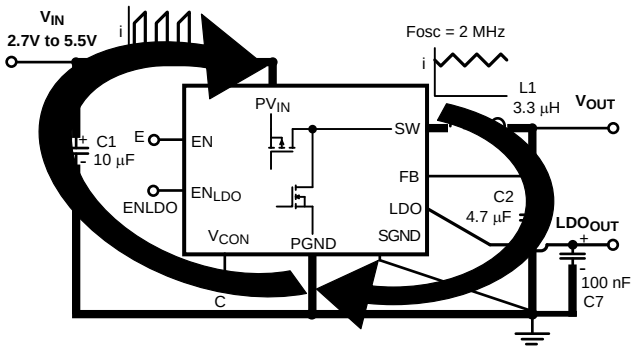

Figure 4. Current Loop

Referring to Figure 4, the LM3207 has two major current loops where pulse and ripple current flow. The loop shown in the left hand side is most important, because pulse current shown in Figure 4 flows in this path. The right hand side is next. The current waveform in this path is triangular, as shown in Figure 4. Pulse current has many high-frequency components due to fast di/dt. Triangular ripple current also has wide high-frequency components. Board layout and circuit pattern design of these two loops are the key factors for reducing noise radiation and stable operation. Other lines, such as from battery to C1(+) and C2(+) to load, are almost DC current, so it is not necessary to take so much care. Only pattern width (current capability) and DCR drop considerations are needed.

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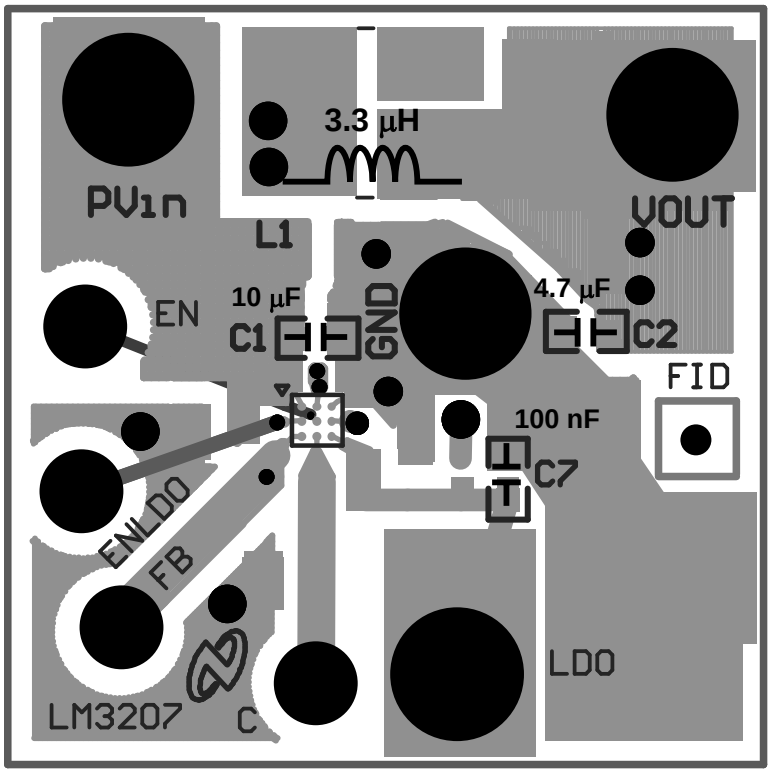

Figure 5. Evaluation Board Layout

BOARD LAYOUT FLOW

1. Minimize C1, PV_{IN}, and PGND loop. These traces should be as wide and short as possible. This is most important.
2. Minimize L1, C2, SW and PGND loop. These traces also should be wide and short. This is the second priority.
3. Above layout patterns should be placed on the component side of the PCB to minimize parasitic inductance and resistance due to via-holes. It may be a good idea that the SW to L1 path is routed between C2(+) and C2(-) land patterns. If vias are used in these large current paths, multiple via-holes should be used if possible.
4. Connect C1(-), C2(-) and PGND with wide GND pattern. This pattern should be short, so C1(-), C2(-), and PGND should be as close as possible. Then connect to a PCB common GND pattern with as many via-holes as possible.
5. SGND should not connect directly to PGND. Connecting these pins under the device should be avoided. (If possible, connect SGND to the common port of C1(-), C2(-) and PGND.)
6. FB line should be protected from noise. It is a good idea to use an inner GND layer (if available) as a shield.
7. The LDO Cap C7 (C_{LDO}) should be placed as close to the PA as possible and as far away from the switcher to suppress high frequency switch noises.

NOTE

The evaluation board shown in Figure 5 for the LM3207 was designed with these considerations, and it shows good performance. However some aspects have not been optimized because of limitations due to evaluation-specific requirements. Please refer questions to a National representative.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LM3207TL-2.53/NOPB	ACTIVE	DSBGA	YZR	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
LM3207TL/NOPB	ACTIVE	DSBGA	YZR	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
LM3207TLX-2.53/NOPB	ACTIVE	DSBGA	YZR	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
LM3207TLX/NOPB	ACTIVE	DSBGA	YZR	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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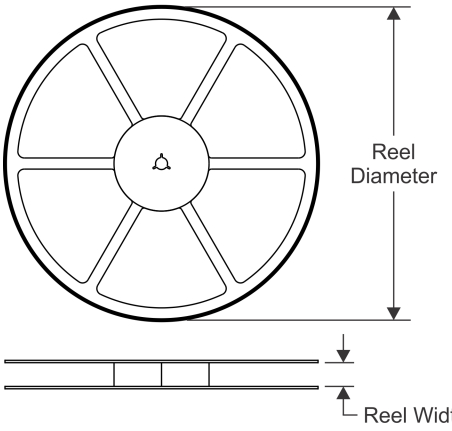
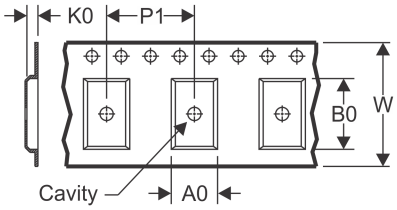
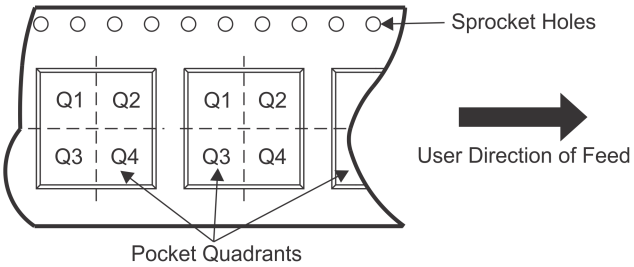


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

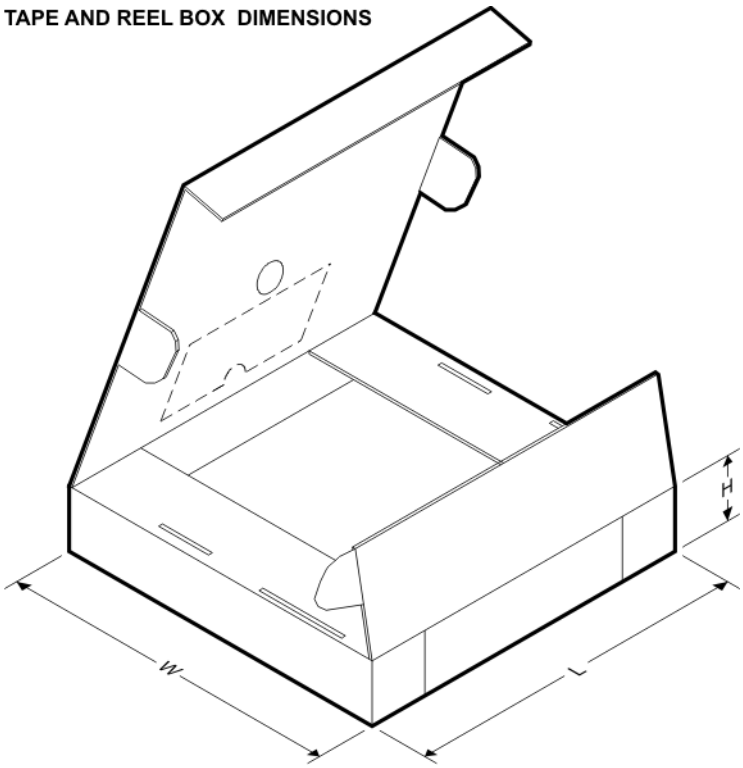
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3207TL-2.53/NOPB	DSBGA	YZR	9	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM3207TL/NOPB	DSBGA	YZR	9	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM3207TLX-2.53/NOPB	DSBGA	YZR	9	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM3207TLX/NOPB	DSBGA	YZR	9	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

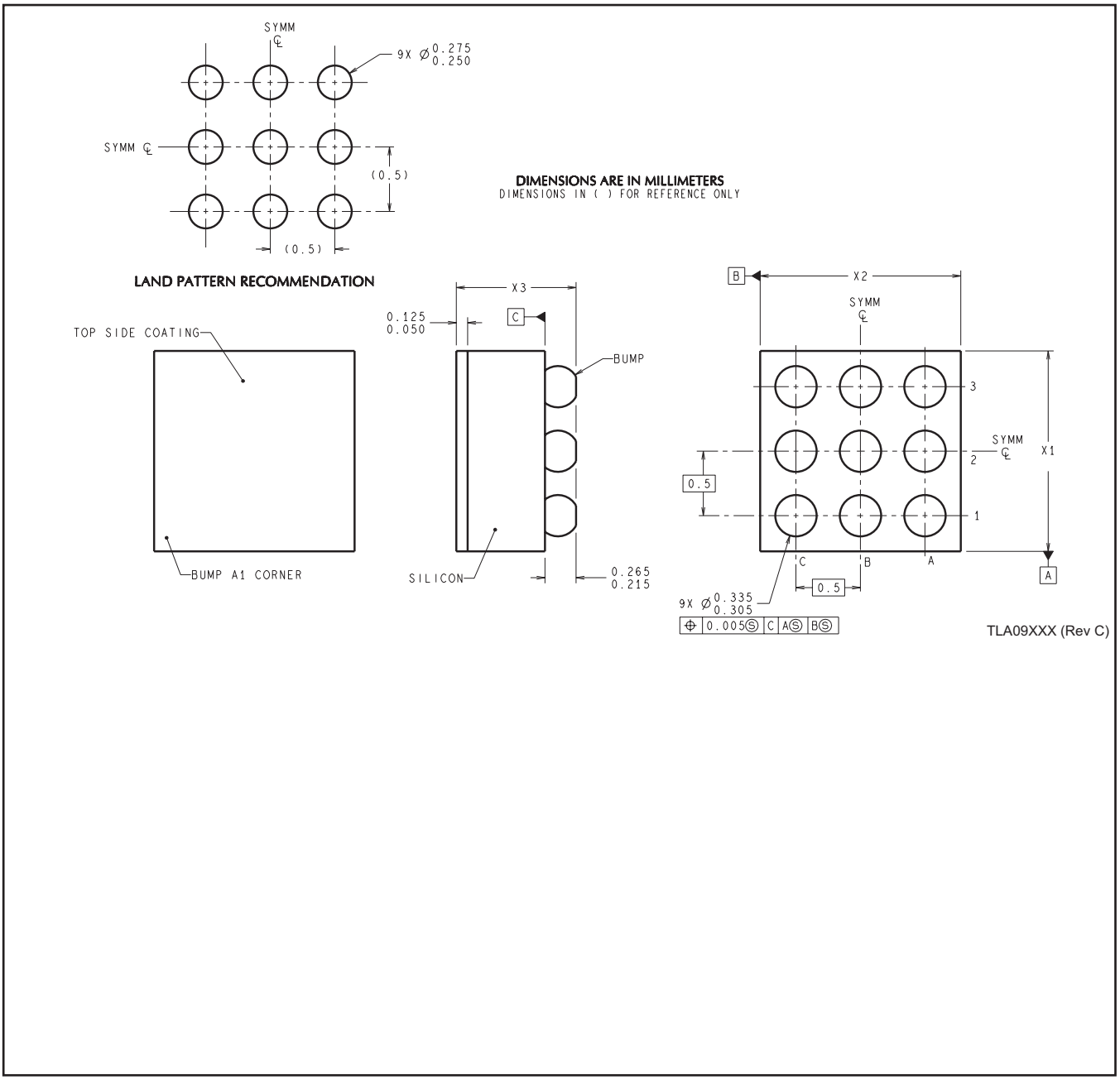
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3207TL-2.53/NOPB	DSBGA	YZR	9	250	203.0	190.0	41.0
LM3207TL/NOPB	DSBGA	YZR	9	250	203.0	190.0	41.0
LM3207TLX-2.53/NOPB	DSBGA	YZR	9	3000	206.0	191.0	90.0
LM3207TLX/NOPB	DSBGA	YZR	9	3000	206.0	191.0	90.0

YZR0009xxx


SYMM
9X Ø 0.275 0.250
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DIMENSIONS IN ( ) FOR REFERENCE ONLY
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X3
0.125 0.050
C
BUMP
SILICON
0.265 0.215
B
X2
SYMM
3
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X1
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